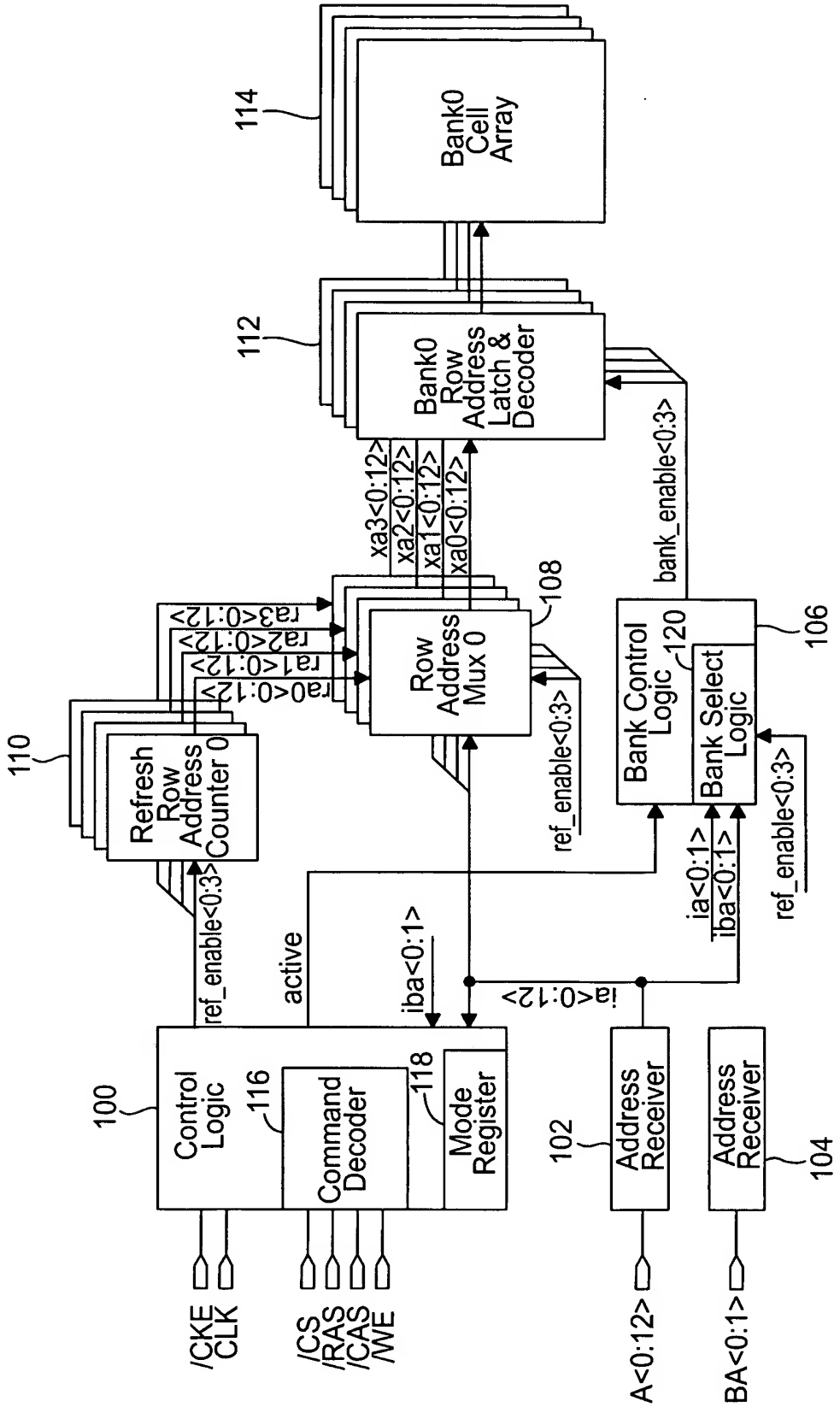
Bank0 Cell Array
114
Bank0 Row Address Latch & Decoder
112
xa3<0:12>
xa2<0:12>
xa1<0:12>
xa0<0:12>
bank_enable<0:3>
108
Row Address Mux 0
ra3<0:12>
ra2<0:12>
ra1<0:12>
ra0<0:12>
110
Refresh Row Address Counter 0
ref_enable<0:3>
Bank Control Logic
120
Bank Select Logic
106
ia<0:1>
iba<0:1>
ref_enable<0:3>
active
iba<0:1>
ia<0:12>
100
Control Logic
116
Command Decoder
118
Mode Register
102
Address Receiver
104
Address Receiver
/CKE
CLK
/CS
/RAS
/CAS
/WE
A<0:12>
BA<0:1>
10

Fig. 1

Bank Selection	BA<0>	BA<1>	A<0>	A<1>
All Banks (BK0,BK1,BK2, BK3)	X	X	1	1
BK0, BK1	X	0	1	0
BK2, BK3	X	1	1	0
BK0, BK2	0	X	0	1
BK1, BK3	1	X	0	1
BK0	0	0	0	0
BK1	1	0	0	0
BK2	0	1	0	0
BK3	1	1	0	0

200

Fig. 2

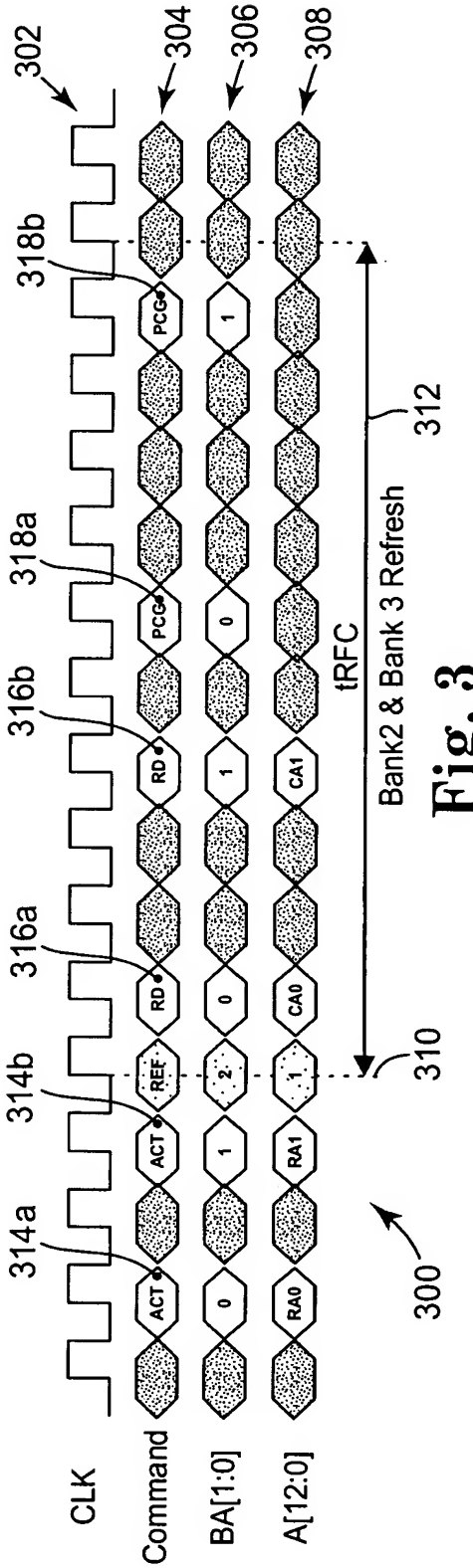

Fig. 3

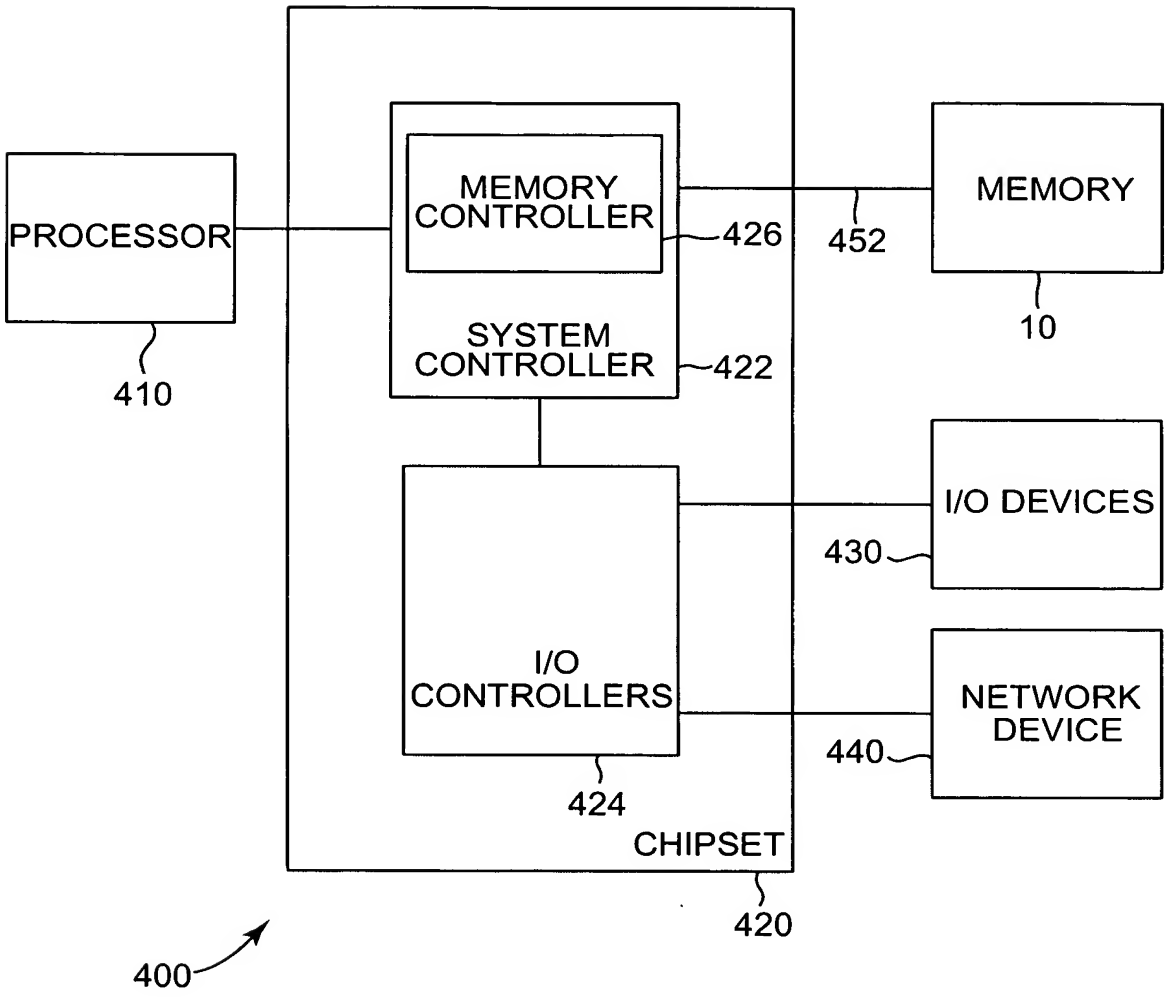
PROCESSOR
410
MEMORY CONTROLLER
426
SYSTEM CONTROLLER
422
452
MEMORY
10
I/O DEVICES
430
I/O CONTROLLERS
424
NETWORK DEVICE
440
CHIPSET
420
400

Fig. 4

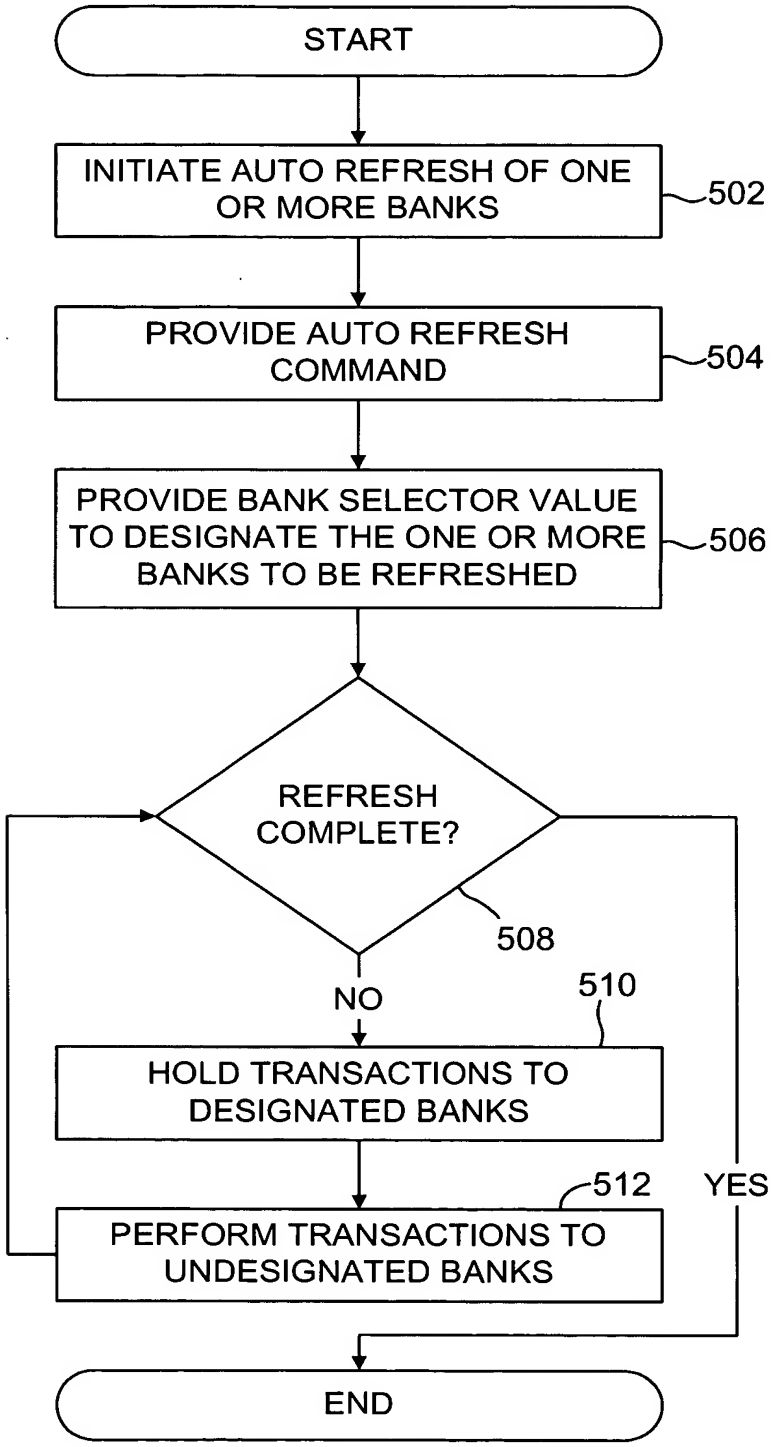
START
INITIATE AUTO REFRESH OF ONE OR MORE BANKS
502
PROVIDE AUTO REFRESH COMMAND
504
PROVIDE BANK SELECTOR VALUE TO DESIGNATE THE ONE OR MORE BANKS TO BE REFRESHED
506
REFRESH COMPLETE?
508
NO
510
HOLD TRANSACTIONS TO DESIGNATED BANKS
512
PERFORM TRANSACTIONS TO UNDESIGNATED BANKS
YES
END

Fig. 5

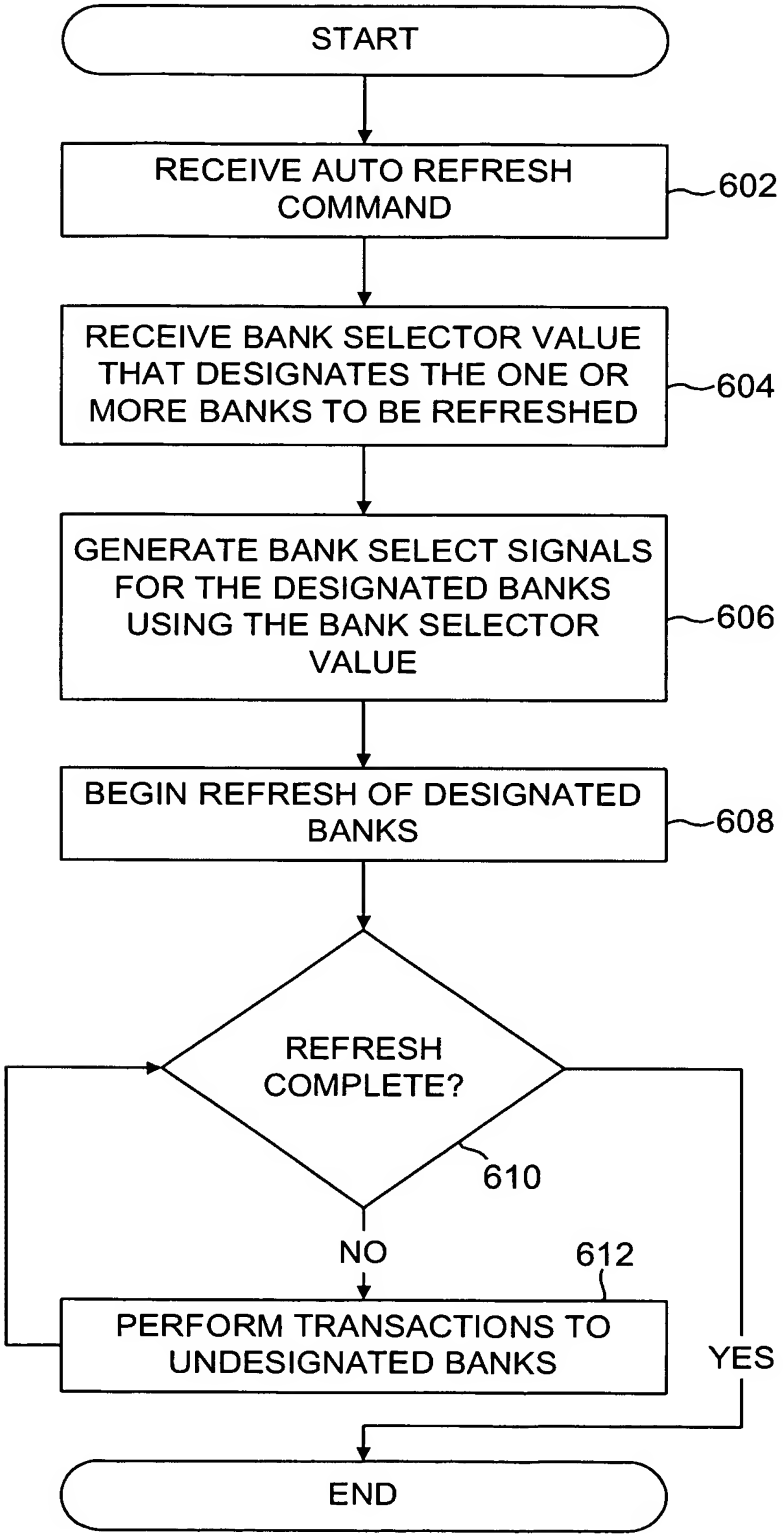
START
RECEIVE AUTO REFRESH COMMAND
602
RECEIVE BANK SELECTOR VALUE THAT DESIGNATES THE ONE OR MORE BANKS TO BE REFRESHED
604
GENERATE BANK SELECT SIGNALS FOR THE DESIGNATED BANKS USING THE BANK SELECTOR VALUE
606
BEGIN REFRESH OF DESIGNATED BANKS
608
REFRESH COMPLETE?
610
NO
612
PERFORM TRANSACTIONS TO UNDESIGNATED BANKS
YES
END

Fig. 6